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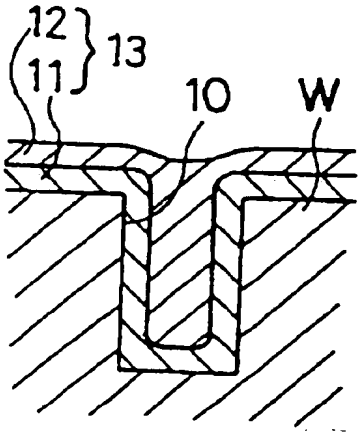
(54) # METHOD AND DEVICE FOR PLATING SUBSTRATE

(57) A method and apparatus for plating a substrate is provided, wherein fine pits formed in the substrate, such as fine channels for wiring, are filled with a copper, copper alloy, or other material with low electrical resistance. The method is performed on a wafer W having fine pits (10) to fill the fine pits with a metal (13) and includes performing a first plating process (11) by immersing the wafer in a first plating solution having a composition superior in throwing power; and performing a second plating process (12) by immersing the substrate in a second plating solution having a composition superior in leveling ability.

FIG. 3C



EP 1 091 024 A1

Description

Technical Field

[0001] The present invention relates to a substrate plating method and apparatus, and particularly to a substrate plating apparatus for filling pits for fine wires and the like formed in a semiconductor wafer with copper or another metal.

Background Art

[0002] Conventionally, wire channels have been formed in a semiconductor wafer by first depositing a conducting layer on the wafer surface using sputtering or a similar technique. Next, the unnecessary portions of the conducting layer are removed through a chemical dry etching process with a pattern mask formed of resist or the like.

[0003] In conventional processes, aluminum (Al) or an aluminum alloy has been used to form the wire circuit. However, wiring has been made thinner to keep up with the increased complexity of semiconductor devices. The increasing current density generates increased thermal stress and higher temperatures. This causes stress-migration or electro-migration, which grow more remarkable as the layers of aluminum or the like are manufactured thinner and give rise to such disorders as wire breakage or short-circuiting.

[0004] To avoid an excessive generation of heat in the wiring, a metal having a higher conductivity such as copper is required to form the wiring.. However, it is difficult to perform dry etching on copper or a copper alloy that has been deposited over the entire surface as in the process described above. An alternative process would be to first form channels for the wiring according to a predetermined pattern and then fill the channels with copper or a copper alloy. This method eliminates the process of removing unnecessary parts of the conductive layer by etching, requiring only that the surface of the wafer be polished to remove uneven areas. The method has the additional benefit of being able to form simultaneously multiple areas called plugs that connect the tops and bottoms of channels.

[0005] However, the shape of these wiring channels and plugs have a considerably high aspect ratio (the ratio of depth to width) as the width of the wiring gets smaller, making it difficult to fill the channels with an even layer of metal using sputtering deposition. The chemical vapor deposition method (CVD) has been used for depositing various materials, but it is difficult to prepare an appropriate gas material for copper or a copper alloy. Further, when using an organic material, carbon from the material becomes mixed in with the deposition layer and increases the resistance.

[0006] Therefore, a method was proposed for performing electroless or electrolytic plating by immersing a substrate into a plating solution. With this method, it is possible to fill wire channels having a high aspect ratio with a uniform layer of metal.

[0007] When performing an electrolytic plating process, for example, generally a plating solution having a composition including copper sulfate and sulfuric acid is used. If the solution has a low concentration of copper sulfate and a high concentration of sulfuric acid, it is known that the plating solution will have high conductivity and great polarization, thereby improving throwing power and coating uniformity. In contrast, if the plating solution has a high concentration of copper sulfate and a low concentration of sulfuric acid, it is known that through the work of an additive the solution will have good leveling ability, in other words, plating will grow from the bottom of the fine pits formed in the substrate surface.

[0008] For this reason, performing a plating process using a plating solution having a composition superior in throwing power and coating uniformity to fill copper in the fine pits of a substrate having a large aspect ratio, the leveling ability of the solution is poor. The inlets of the fine pits will be blocked first before the pits are filled, thereby tending to form voids in the pits. On the other hand, using a plating solution with a composition superior in leveling ability will be inferior in throwing power and coating uniformity, resulting in unplated areas on the walls and bottoms of the fine pits.

[0009] Generally in these plating processes, a copper seed layer is formed on the bottom surface and area surrounding the fine pits of the substrate. However, when performing electrolytic plating directly on a barrier layer, such as TiN or TaN, the sheet resistance of the barrier layer is much larger than the resistance of the copper sulfate plating solution. As a result, needle-shaped crystals are formed in plating processes using copper sulfate solution, resulting in a plating layer having loose adherence.

[0010] In addition a copper pyrophosphate plating solution is also widely used because of its close adhesion due to high polarization and layered deposition property. However, copper pyrophosphate plating solution has poor leveling ability. Hence, when filling fine pits with copper in a plating process using copper pyrophosphate plating solution, the inlets to the fine pits become blocked first, thereby developing voids, as described above. Of course, it is also possible to use copper pyrophosphate plating solution as a first layer over a copper seed layer.

Disclosure of Invention

[0011] In view of the foregoing, it is an object of the present invention to provide a method and apparatus of plating a substrate capable of filling fine pits of channels and the like for fine wiring with copper, a copper alloy, or similar material having a low electrical resistance, such that the plating is uniform with no gaps and has a smooth surface.

[0012] These objects and others will be attained by a method for plating a substrate having a surface with fine pits formed therein, the method comprising; performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power; and performing a second plating process by immersing the substrate in a second plating solution having a composition superior in leveling ability.

[0013] With this method, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pits is formed in the first plating process. A surface plating layer having a smooth surface and no void is formed on top of the initial plating layer in the second plating process.

[0014] According to another aspect of the present invention, the first plating solution is a high throwing power copper sulfate plating solution for printed circuit boards and the second plating solution is a copper sulfate solution. The high throwing power copper sulfate plating solution has a low concentration of copper sulfate, a high concentration of sulfuric acid, and is therefore superior in throwing power and coating uniformity. The copper sulfate plating solution has a high concentration of copper sulfate and a low concentration of sulfuric acid and is superior in leveling ability. As a result, plating metal is uniformly deposited on the surface of the semiconductor wafer, eliminating unplated areas formed on the side and bottom surfaces of the fine pits.

[0015] According to another aspect of the present invention, the high throwing power copper sulfate plating solution has a composition of 5-100 g/l of copper sulfate and 100-250 g/l of sulfuric acid, and the copper sulfate solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

[0016] According to another aspect of the present invention, a method for plating a substrate having a surface with fine pits formed therein and coated with a barrier layer, comprises; performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power and in closely adhering to the barrier layer; and performing a second plating process by immersing the substrate in a second plating solution having a composition superior in leveling ability.

[0017] With this method, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pits covered by the barrier layer is formed in the first plating process. A surface plating layer having a smooth surface and no void is formed on top of the initial plating layer in the second plating process.

[0018] According to another aspect of the present invention, the first plating solution is a copper pyrophosphate solution for printed circuit boards and the second plating solution is a copper sulfate solution. Due to the high polarization and the layered deposition property, the copper pyrophosphate sulfate solution forms a coating in close adherence with the barrier layer 5 formed of TiN or the like. The copper sulfate plating solution having a high concentration of copper sulfate and a low concentration of sulfuric acid is superior in leveling ability. Hence, this process forms a plating layer free of voids in the fine pits covered by the barrier layer, and the surface of the plating layer is smooth.

[0019] According to another aspect of the present invention, the copper sulfate solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

[0020] According to another aspect of the present invention, a substrate plating apparatus comprises a plating bath; first plating solution supplying means for supplying a first plating solution having a composition superior in throwing power to the plating bath; second plating solution supplying means for supplying a second plating solution having a composition superior in leveling ability to the plating bath; and switching means for switching on and off the plating solutions supplied front the first and second plating solution supplying means.

[0021] With this construction, both the first and second plating processes can be performed in the same apparatus, since supply of plating solution is switched between processes, from the first plating solution superior in throwing power to the second plating solution superior in leveling.

[0022] According to another aspect of the present invention, the first plating solution has a composition with qualities superior for close adherence to a barrier layer formed on the surface of the substrate. With this construction, both the first and second plating processes can be performed in the same apparatus, since supply of plating solution is switched between processes, from the first plating solution superior in adherence to the barrier layer to the second plating solution superior in leveling.

Brief Description of Drawings

[0023]

Figs. 1A-1C are cross-sectional diagrams showing the process for manufacturing a semiconductor element according to the substrate plating method of the present invention;

Fig. 2 is a flowchart showing the process of the plating method of the preferred embodiment;

Figs. 3A-3C are cross-sectional diagrams illustrating the process of Fig. 2;

Figs. 4A-4B are cross-sectional diagrams illustrating leveling ability;

Fig. 5 shows the general construction of a plating apparatus according to the preferred embodiment;

Figs. 6A-6C are cross-sectional diagrams showing the differences based on first and second comparisons to the first embodiment;

Figs. 7A-7C are cross-sectional diagrams illustrating the process of the plating method according to

the second embodiment;

Figs. 8A-8C are cross-sectional diagrams showing the differences based on first and second comparisons to the second embodiment; and

Fig. 9 is a flowchart showing the plating process employing a variation of the plating apparatus shown in Fig. 5.

Best Mode for Carrying Out the Invention

[0024] A substrate plating method and apparatus according to preferred embodiments of the present invention will be described while referring to the accompanying drawings.

[0025] A substrate plating method according to a first embodiment forms a copper plating on the surface of a semiconductor wafer in order to obtain a semiconductor device having wiring formed from the copper layer. This process is described with reference to Figs. 1A-1C.

[0026] As shown in Fig. 1A, a semiconductor wafer W is formed of a semiconductor material 1, a conducting layer 1a formed on the top surface of the semiconductor material 1, and an SiO_2 insulating layer 2 deposited on top of the conducting layer 1a. A contact hole 3 and a channel 4 are formed in the insulating layer 2 by a lithography etching technique. A barrier layer 5, such as TiN, is formed over the surfaces in the contact hole 3 and channel 4.

[0027] By performing a copper plating process on the surface of the semiconductor wafer W, the contact hole 3 and channel 4 are filled with a copper layer 6. The copper layer 6 is also deposited on top of the insulating layer 2. Next, chemical mechanical polishing (CMP) is performed to remove the copper layer 6 from the top of the insulating layer 2. This process is necessary to form the surface on the copper layer 6 filling the contact hole 3 and channel 4 to be approximately flush with the surface of the insulating layer 2. As a result, the copper layer 6 forms wiring, as shown in Fig. 1C.

[0028] Next, an electrolytic plating process for plating the semiconductor wafer W shown in Fig. 1A will be described with reference to Fig. 2. First, a preprocess is performed. In the preprocess, the semiconductor wafer W is immersed in an aqueous sulfuric acid solution to activate the semiconductor wafer W.

[0029] After washing the semiconductor wafer W, a first plating process is performed by immersing the semiconductor wafer W into a first plating solution, such as a high throwing power copper sulfate plating solution used for printed circuit boards. As shown in Fig. 3A, this process forms a uniform initial plating layer 11 over the surface of a fine pit 10 formed in the semiconductor wafer W, wherein the surface includes the bottom and side walls of the fine pit 10. Here, the high throwing power copper sulfate solution has a low concentration of copper sulfate, a high concentration of sulfuric acid, and is superior in throwing power and coating uniformity. An example composition of this solution is 5-100 g/l of copper sulfate and 100-250 g/l of sulfuric acid.

[0030] Since the plating solution has a low concentration of copper sulfate and a high concentration of sulfuric acid, the conductivity of the solution is high and the polarization is great, thereby improving throwing power. As a result, plating metal is uniformly deposited on the surface of the semiconductor wafer W, eliminating unplated areas formed on the side and bottom surfaces of the fine pit 10.

[0031] After again washing the semiconductor wafer W, a second plating process is performed by immersing the semiconductor wafer W into a second plating solution, such as a copper sulfate plating solution for decorative uses. As shown in Figs. 3B and 3C, this process forms a plating layer 12 having a flat surface on the surface of the initial plating layer 11. Here, the copper sulfate plating solution has a high concentration of copper sulfate and a low concentration of sulfuric acid and is superior in leveling ability. An example composition of the solution is 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

[0032] Here, leveling ability defines a quality describing the degree of smoothness on the plating surface. With good leveling ability, it is possible to obtain a plating layer 15a having a flat surface, as shown in Fig. 4A, even when a depression 14 is formed in the surface of the semiconductor wafer W. With a poor leveling ability, however, a plating layer 15b, as shown in Fig. 4B, is obtained. Here, the shape of the depression 14 formed in the surface of the semiconductor wafer W is reflected in the plating layer 15b.

[0033] Hence, when using a plating solution having superior leveling ability, film at the inlet to the fine pit 10 grows slow, as shown in Fig. 3B. This slow growth can prevent the generation of voids, thereby filling the fine pit 10 with a uniform layer of copper plating having no gaps. Moreover, it is possible to achieve a smooth surface on the plating.

[0034] Subsequently, the semiconductor wafer W is washed and dried to complete the plating process. This process achieves a plating layer 13 having a flat surface and free of voids. The fine pit 10 contains no unplated areas on its bottom or side walls.

[0035] Fig. 5 shows the construction of a plating apparatus suitable for the plating process described above.

[0036] The plating apparatus is provided with a plating bath 20; a first plating solution supplying section 22a for supplying a first plating solution 21 into the plating bath 20; and a second plating solution supplying section 22b for supplying a second plating solution 23 into the plating bath 20.

[0037] The first plating solution supplying section 22a includes a pump 24a for pumping first plating solution 21 into the plating bath 20; a shut-off valve 25a disposed upstream from the pump 24a; and a timer 26a for opening and closing the shut-off valve 25a.

[0038] Similarly, the second plating solution supplying section 22b includes a pump 24b for pumping second plating solution 23 into the plating bath 20; a shut-off valve 25b disposed upstream from the pump 24b; and a timer 26b for opening and closing the shut-off valve 25b.

[0039] In addition, a wash water supply tube 27 and a discharge tube 28 are connected to the plating bath 20 for introducing wash water into the plating bath 20 and discharging wash water out of the plating bath 20, respectively. A pump 29 is connected to the tube 28.

[0040] As described above, a semiconductor wafer W having undergone a preprocess, is inserted into the plating bath 20. Wash water is introduced into the plating bath 20 and the semiconductor wafer W is washed. Next, the shut-off valve 25a is opened according to the timer 26a. The first plating solution 21 is supplied into the plating bath 20, and the first plating process is performed. After a fixed time has elapsed, the shut-off valve 25a is closed. Wash water is again introduced into the plating bath 20 for washing the semiconductor wafer W. Subsequently, the shut-off valve 25b of the second plating solution supplying section 22b is opened according to timer 26b. The second plating solution 23 is supplied into the plating bath 20 and the second plating process is performed. Accordingly, it is possible to perform both the first and second plating processes consecutively using the same apparatus.

[0041] In the example described above, a timer is used for switching the supply of plating solution on and off. However, it is obvious that any means capable of performing this process can be used.

[0042] In the example described above, the same processing tank is used for performing the first plating process, the second plating process, and the washing processes. However, these processes can be performed using separate baths for each process. As shown in Fig. 9, for example, multiple baths can be provided, wherein the plating process is performed by immersing the semiconductor wafer W into each bath in order according to each step of the process.

(First Embodiment)

[0043] In the first embodiment, the fine pit 10 having a width of 1.0 μm or less is formed on the semiconductor wafer W. An aqueous solution having 100 g/l of sulfuric acid is maintained at a temperature of 50°C. A preprocess is performed by immersing the semiconductor wafer W into the aqueous solution for 15 seconds. Subsequently, the first plating process is performed with the first plating solution and, after washing the semiconductor wafer W, the second plating process is performed using the second plating solution. The semiconductor wafer W is then washed and dried.

[0044] Here, the composition of the first plating solution is as follows.

$CuSO_4 \cdot 5H_2O$	70 g/l
H_2SO_4	200 g/l
NaCl	100 mg/l
Organic additive	5 ml/l

[0045] The composition of the second plating solution is as follows.

$CuSO_4 \cdot 5H_2O$	200 g/l
H_2SO_4	50 g/l
NaCl	100 mg/l
Organic additive	5 ml/l

[0046] The conditions for the plating processes, described below, are the same for both processes.

Bath temperature	25°C
Current density	2 A/dm^2
Plating time	2.5 min.
PH < 1	

[0047] This process forms the plating layer 13 free of voids in the fine pit 10, as shown in Fig. 6A. No unplated areas are developed in the fine pit 10.

(First Comparison)

[0048] In a first comparison to the first embodiment, a semiconductor wafer W having undergone the same preprocess described above is plated using only the first plating solution. As shown in Fig. 6B, a void 30 is formed in the plating layer 13 within the fine pit 10.

(Second Comparison)

[0049] In a second comparison to the first embodiment, a semiconductor wafer W having undergone the same preprocess described above is plated using only the second plating solution. As shown in Fig. 6C, an unplated area 31 exists in a bottom corner of the fine pit 10.

[0050] Next, a second embodiment of the present invention will be described.

[0051] As shown in Fig. 1A, a semiconductor wafer W is formed of a semiconductor material 1, a conduct-

ing layer 1a formed on the top surface of the semiconductor material 1, and an SiO_2 insulating layer 2 deposited on top of the conducting layer 1a. A contact hole 3 and a channel 4 are formed in the insulating layer 2 by a lithography etching technique. A barrier layer 5, such as TiN, is formed over the surfaces in the contact hole 3 and channel 4.

[0052] First, a preprocess is performed. In the preprocess, the semiconductor wafer W is immersed in an aqueous sulfuric acid solution to activate the semiconductor wafer W. After washing the semiconductor wafer W, a first plating process is performed by immersing the semiconductor wafer W into a first plating solution, such as a copper pyrophosphate solution. As shown in Fig. 7A, this process forms a uniform initial plating layer 11 over the surface including the barrier layer 5. The barrier layer 5 covers the bottom and side walls of a fine pit 10 formed in the semiconductor wafer W.

[0053] Here, the copper pyrophosphate sulfate solution forms a layered deposition providing superior close adherence with the barrier layer 5. Hence, this process forms an initial plating layer 11a having a throwing power and prevents the generation of unplated areas on the barrier layer 5 covering the fine pit 10.

[0054] After washing the semiconductor wafer W, a second plating process is performed by immersing the semiconductor wafer W into a second plating solution, such as a copper sulfate plating solution. As shown in Figs. 7B and 7C, this process forms a plating layer 12 having a flat surface on the surface of the initial plating layer 11a. Here, the copper sulfate plating solution has a high concentration of copper sulfate and a low concentration of sulfuric acid and is superior in leveling ability. An example composition of the solution is 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

(Second Embodiment)

[0055] In the second embodiment, the fine pit 10 having a width of 1.0 μm or less is formed on the semiconductor wafer W. The barrier layer 5 covers the fine pit 10. An aqueous solution having 100 g/l of sulfuric acid is maintained at a temperature of 50°C. A preprocess is performed by immersing the semiconductor wafer W into the aqueous solution for 15 seconds. Subsequently, the first plating process is performed with the first plating solution and, after washing the semiconductor wafer W, the second plating process is performed using the second plating solution. The semiconductor wafer W is then washed and dried.

[0056] Here, the composition of the first plating solution is as follows.

$Cu_2P_2O_7 \cdot 3H_2O$	90 g/l
$H_4P_2O_7$	340 g/l
Ammonia	3 ml/l
Organic additive	0.5 ml/l

[0057] The conditions for the plating process are as follows.

Bath temperature	55°C
Current density	0.5 A/dm^2
Plating time	3 min.
PH 8.5	

[0058] The composition of the second plating solution is as follows.

$CuSO_4 \cdot 5H_2O$	200 g/l
H_2SO_4	50 g/l
NaCl	100 mg/l
Organic additive	5 ml/l

[0059] The conditions for the plating process are as follows.

Bath temperature	25°C
Current density	2 A/dm^2
Plating time	2.5 min.
PH < 1	

[0060] This process forms a plating layer 14 free of voids in the fine pit 10, as shown in Fig. 8A. No unplated areas are developed on the barrier layer 5 within the fine pit 10.

(First Comparison)

[0061] In a first comparison to the first embodiment, a semiconductor wafer W having undergone the same preprocess described above is plated using only the first plating solution. As shown in Fig. 8B, a void 30 is formed in the plating layer 14 within the fine pit 10.

(Second Comparison)

[0062] In a second comparison to the first embodiment, a semiconductor wafer W having undergone the

same preprocess described above is plated using only the second plating solution. As shown in Fig. 8C, an unplated area 31 exists on the barrier layer 5 in a bottom corner of the fine pit 10.

[0063] In the first plating process of the present invention described above, a uniform initial plating layer without unplated areas on the side walls and bottom of the fine pit 10 is formed. In the second plating process of the present invention, a surface plating layer having a smooth surface and no void is formed on top of the initial plating layer. Accordingly, fine pits formed in the substrate, such as fine channels for wiring, can be filled with a copper, copper alloy, or other material having low electrical resistance without gaps in the metal plating and with an level surface.

Industrial Applicability

[0064] The present invention is a plating process capable of forming embedded wiring layers and the like in semiconductor wafers and can be applied to the fabrication of LSI chips and other semiconductor devices.

Claims

1. A method for plating a substrate having a surface with fine pits formed therein, the method comprising:

   performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power; and
   performing a second plating process by immersing the substrate in a second plating solution having a composition superior in leveling ability.

2. A method for plating a substrate as claimed in claim 1, wherein the first plating solution is a high throwing power copper sulfate plating solution for printed circuit boards and the second plating solution is a copper sulfate plating solution.

3. A method for plating a substrate as claimed in claim 2, wherein the high throwing power copper sulfate plating solution has a composition of 5-100 g/l of copper sulfate and 100-250 g/l of sulfuric acid, and the copper sulfate plating solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

4. (amended) A method for plating a substrate having a surface with fine pits formed therein and coated with a barrier layer, comprising the steps of:

   performing a first plating process by immersing the substrate in a first plating solution having a composition superior in throwing power and in close adherence; and
   performing a second plating process by immersing the substrate in a second plating solution having a composition superior in leveling ability.

5. A method for plating a substrate as claimed in claim 4, wherein the first plating solution is a copper pyrophosphate plating solution for printed circuit boards and the second plating solution is a copper sulfate plating solution.

6. A method for plating a substrate as claimed in claim 5, wherein the copper sulfate plating solution has a composition of 100-300 g/l of copper sulfate and 10-100 g/l of sulfuric acid.

7. A substrate plating apparatus comprising:

   a plating bath;
   first plating solution supplying means for supplying a first plating solution having a composition superior in throwing power to the plating bath;
   second plating solution supplying means for supplying a second plating solution having a composition superior in leveling ability to the plating bath; and
   switching means for switching on and off the plating solutions supplied from the first and second plating solution supplying means.

8. A substrate plating apparatus as claimed in claim 7, wherein the first plating solution has a composition with qualities superior for close adherence to a barrier layer formed on the surface of the substrate.

FIG. 1A

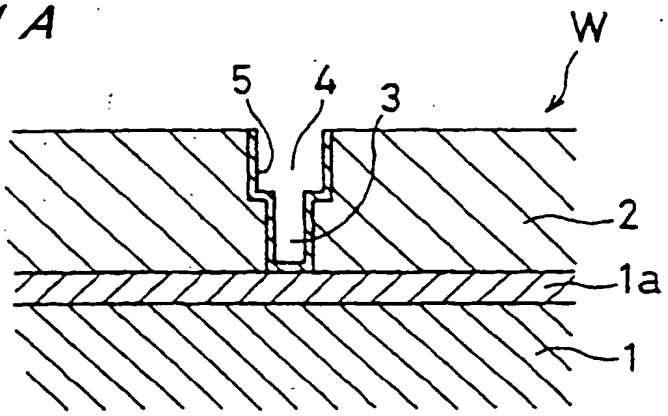


FIG. 1B

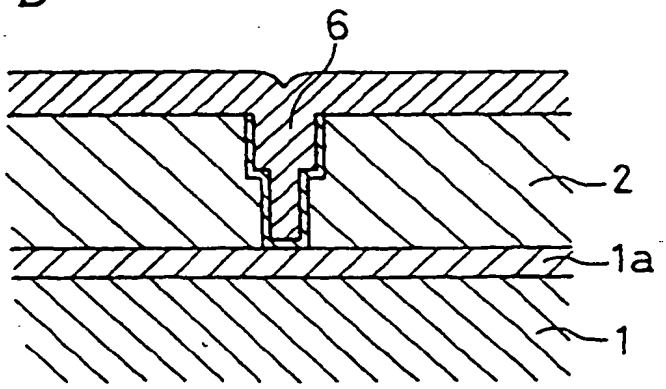


FIG. 1C

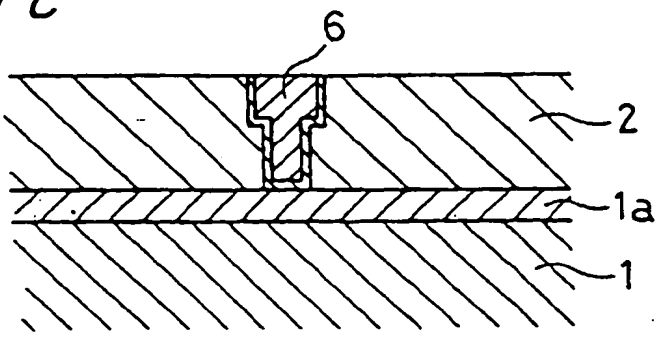


FIG. 2

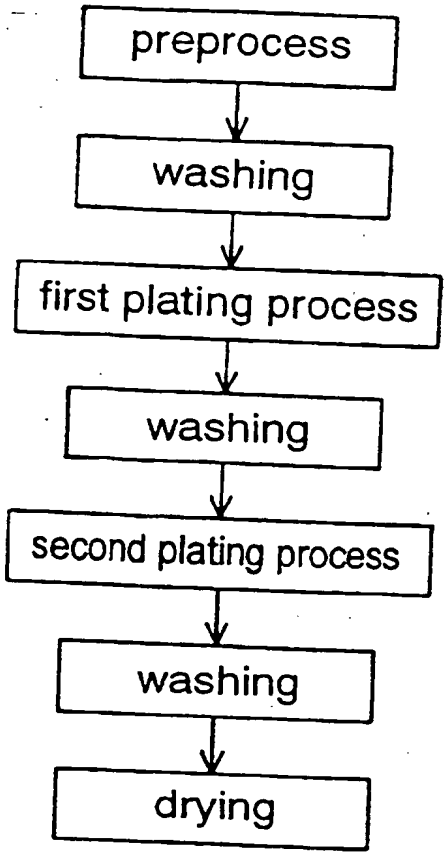


FIG. 3A

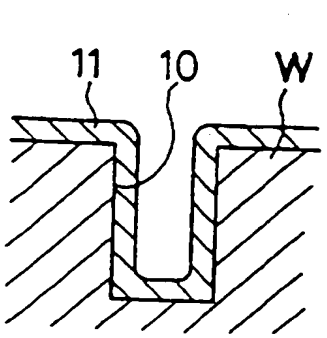


FIG. 3B

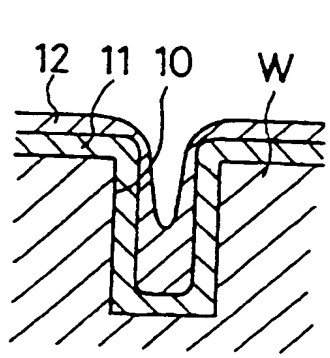


FIG. 3C

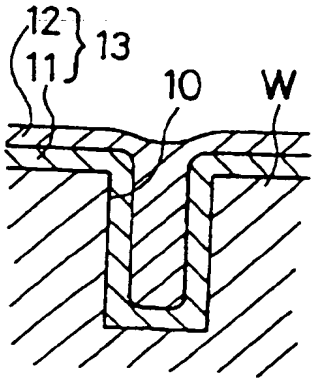


FIG. 4A

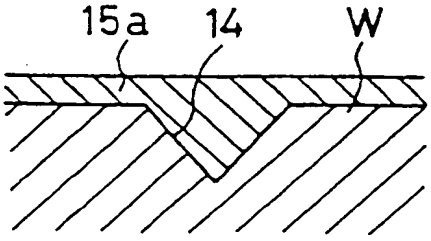


FIG. 4B

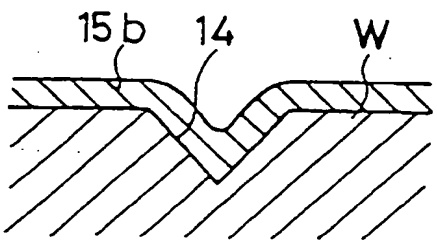


FIG. 5

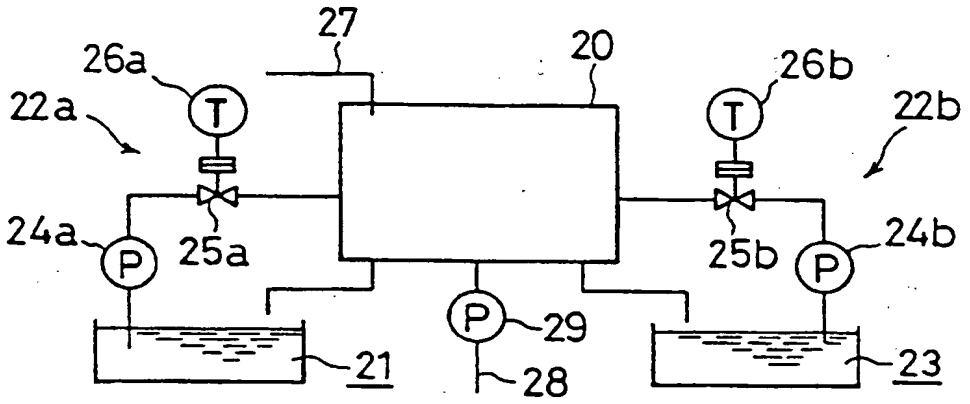


FIG. 6A

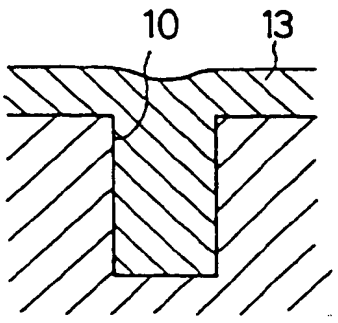


FIG. 6B

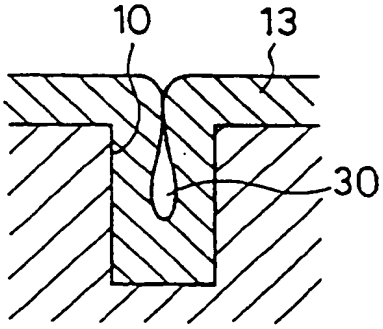


FIG. 6C

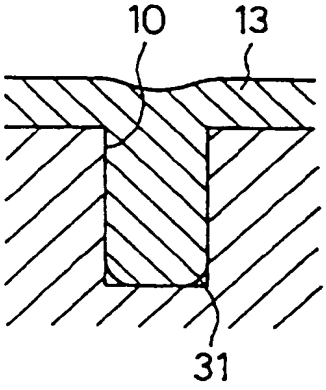


FIG. 7A

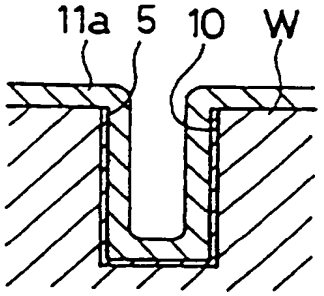


FIG. 7B

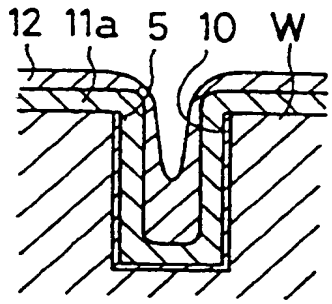


FIG. 7C

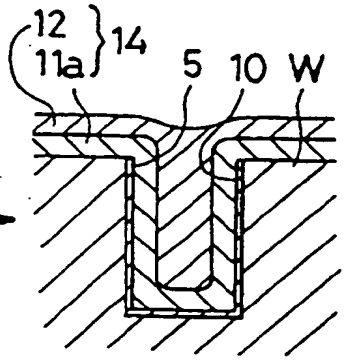


FIG. 8A

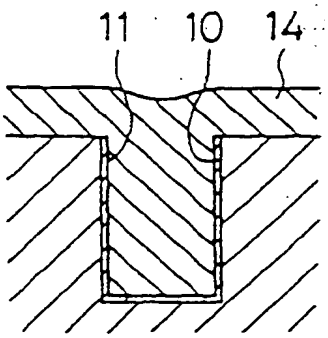


FIG. 8B

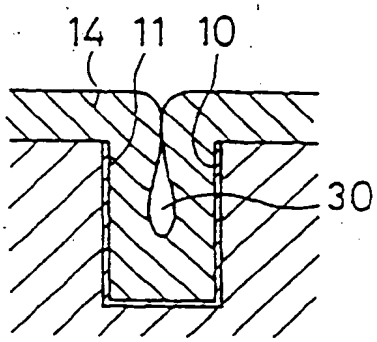


FIG. 8C

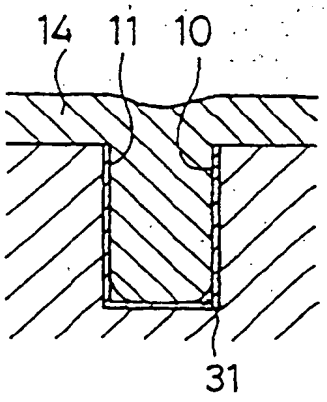
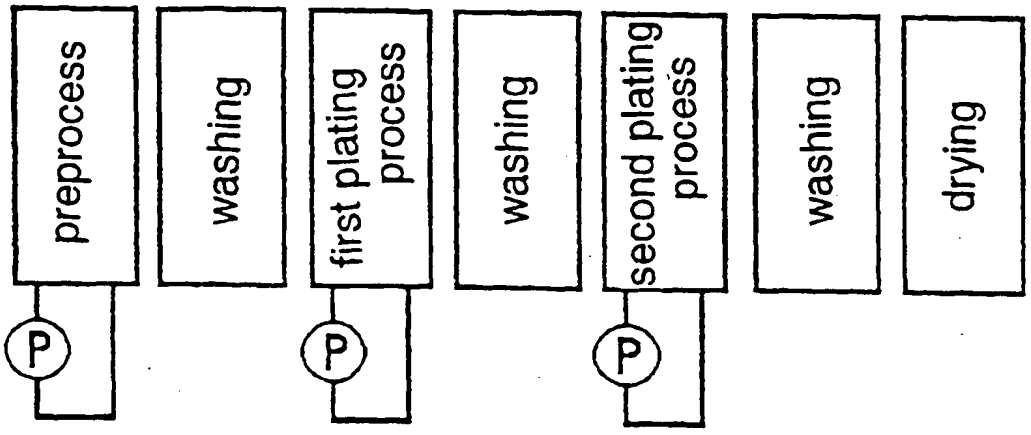


FIG. 9



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/02271

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl⁶ C25D7/12, 7/10, 5/10, 3/38, 101, 5/34, H05K1/18, 3/24, 3/18, H01L21/288, 21/88
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED
Minimum documentation searched (classification system followed by classification symbols)
Int.Cl⁶ C25D1/00-7/12, H05K1/18-3/26, H01L21/288, 21/88

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Toroku Jitsuyo Shinan Koho 1994-1999
Kokai Jitsuyo Shinan Koho 1971-1999 Jitsuyo Shinan Toroku Koho 1996-1999

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP, 5-140795, A (Toagosei Kagaku Kogyo K.K.), 8 June, 1993 (08. 06. 93), Page 2, right column, lines 25 to 38 ; page 3, left column, line 20 to page 4, right column, line 46 (Family: none)	1-6, 7-8
X A	JP, 62-276893, A (Meiko Electronics Co., Ltd.), 1 December, 1987 (01. 12. 87), Page 1, lower left column, line 5 to page 2, upper left column line 14 ; page 7, upper right column, line 11 to lower left column, line 3 & WO, 8705182, A	1-4, 5-8
X A	JP, 53-53527, A (Furukawa Kinzoku Kogyo K.K.), 16 May, 1978 (16. 05. 78), Page 1, lower left column, lines 5 to 13 ; page 2, lower left column, line 17 to page 3, upper right column, line 20 (Family: none)	1-6, 7-8

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
2 August, 1999 (02. 08. 99)	10 August, 1999 (10. 08. 99)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP99/02271

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X A	JP, 53-143971, A (Hitachi,Ltd.), 14 December, 1978 (14. 12. 78), Page 1, lower left column, line 4 to page 3, lower right column, line 2 (Family: none)	1-6, 7-8
X X A A	JP, 07-41991, A (Totoku Electric Co., Ltd.), 10 February, 1995 (10. 02. 95), Page 2, left column, line 2 to right column, line 18 ; Figs. 1, 4 (Family: none)	1, 4, 7-8, 2-3, 5-6

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